

**Unit - I****Chapter 1 : Logic Gates & Boolean Algebra 1-1 to 1-22**

Syllabus : Logic gates : Symbol, Diode/Transistor switch circuit and logical expression, Truth table of basic gates (AND, OR, NOT), Universal gates (NAND and NOR) and special purpose gates (EX-OR, EX-NOR), Boolean algebra : Laws of Boolean algebra, Duality theorem, De-Morgan's theorems.

| | | |
|-------|--|-----|
| 1.1 | Introduction | 1-1 |
| 1.1.1 | NOT Operator (Inversion) | 1-1 |
| 1.1.2 | AND Operator | 1-1 |
| 1.1.3 | OR Operator | 1-1 |
| 1.1.4 | Logic Gates | 1-1 |
| 1.1.5 | Gates, Symbols and Boolean Expression | 1-2 |
| 1.2 | Boolean (Binary) Algebra | 1-2 |
| 1.3 | Boolean Laws | 1-2 |
| 1.3.1 | Commutative Law | 1-3 |
| 1.3.2 | Associative Law | 1-3 |
| 1.3.3 | Distributive Law | 1-3 |
| 1.3.4 | AND Laws | 1-3 |
| 1.3.5 | OR Laws | 1-3 |
| 1.3.6 | INVERSION Law | 1-3 |
| 1.3.7 | Other Important Rules | 1-4 |
| 1.3.8 | Principle of Duality | 1-4 |
| 1.3.9 | Duality Theorem | 1-4 |
| 1.4 | De-Morgan's Theorems | 1-5 |
| 1.4.1 | Examples on Simplification of Logic Expression | 1-5 |

| | | |
|--------|---|------|
| 1.5 | Logic Gates | 1-7 |
| 1.5.1 | Classification of Logic Gates | 1-7 |
| 1.6 | NOT Gate or Inverter | 1-7 |
| 1.6.1 | NOT Gate Using Switches | 1-7 |
| 1.6.2 | NOT Gate using Transistor | 1-7 |
| 1.7 | AND Gate | 1-8 |
| 1.7.1 | AND Gate Using Switches | 1-8 |
| 1.7.2 | AND Gate Using Diodes | 1-8 |
| 1.8 | The OR Gate | 1-9 |
| 1.8.1 | OR Gate Using Switches | 1-9 |
| 1.8.2 | OR Gate using Diodes | 1-9 |
| 1.9 | The NAND Gate | 1-10 |
| 1.10 | The NOR Gate | 1-10 |
| 1.11 | EX-OR and EX-NOR Gates | 1-11 |
| 1.11.1 | The EX-OR Gate | 1-11 |
| 1.11.2 | The EX-NOR Gate | 1-11 |
| 1.12 | Writing Boolean Expression from a Logic Diagram | 1-11 |
| 1.13 | Construction of a Logic Circuit from the Given Boolean Expression | 1-12 |
| 1.14 | Gates using More than 2 Inputs | 1-13 |
| 1.14.1 | Multiple Input AND Gates | 1-13 |
| 1.14.2 | Multiple Input OR Gate | 1-14 |
| 1.14.3 | Multiple Input NAND Gate | 1-14 |
| 1.14.4 | Multiple Input NOR Gate | 1-14 |
| 1.14.5 | Multiple Input EX-OR Gate | 1-15 |
| 1.14.6 | Multiple Input EX-NOR Gate | 1-15 |
| 1.15 | Universal Gates | 1-16 |



| | | |
|--------|--------------------------------------|-------------|
| 1.15.1 | NAND Gate as a Universal Gate | 1-16 |
| 1.15.2 | NOR Gate as a Universal Gate | 1-17 |
| 1.16 | TTL and CMOS Logic Gate ICs | 1-20 |
| 1.17 | I-Scheme Solved Examples..... | 1-21 |
| 1.18 | I-Scheme Questions and Answers | 1-22 |
| • | Review Questions | 1-20 |

Unit - I**Chapter 2 : Logic Families 2-1 to 2-13**

Syllabus : Logic families : Characteristics of logic families : Noise margin, Power dissipation, Figure of merit, Fan-in and Fan-out, Speed of operation, Comparison of TTL, CMOS, ECL, Types of TTL NAND gate.

| | | |
|-------|--|-----|
| 2.1 | Logic Families | 2-1 |
| 2.2 | Classification of Logic Families | 2-1 |
| 2.2.1 | Classification Based on Devices Used ... | 2-1 |
| 2.2.2 | Classification Based on Circuit | |
| | Complexity | 2-2 |
| 2.3 | Characteristics of Digital ICs | 2-2 |
| 2.3.1 | Voltage and Current Parameters | 2-2 |
| 2.3.2 | Fan-in and Fan-out | 2-3 |
| 2.3.3 | Noise Margin | 2-3 |
| 2.3.4 | Propagation Delay | |
| | (Speed of Operation)..... | 2-3 |
| 2.3.5 | Power Dissipation | 2-4 |
| 2.3.6 | Operating Temperature | 2-4 |
| 2.3.7 | Figure of Merit | |
| | (Speed Power Product SPP) | 2-4 |
| 2.3.8 | Invalid Voltage Levels | 2-4 |
| 2.3.9 | Current Sourcing and Current Sinking ... | 2-4 |

| | | |
|--------|---|------|
| 2.4 | TTL Family | 2-5 |
| 2.4.1 | Standard TTL Characteristics | 2-5 |
| 2.4.2 | Advantages of TTL | 2-6 |
| 2.4.3 | Disadvantages of TTL | 2-6 |
| 2.5 | CMOS Logic | 2-6 |
| 2.5.1 | CMOS Characteristics | 2-6 |
| 2.6 | Advantages and Disadvantages of CMOS | 2-6 |
| 2.6.1 | Advantages of CMOS | 2-6 |
| 2.6.2 | Disadvantages of CMOS | 2-6 |
| 2.7 | Emitter Coupled Logic (ECL) | 2-6 |
| 2.7.1 | ECL Characteristics | 2-7 |
| 2.7.2 | Advantages and Disadvantages of ECL Family | 2-7 |
| 2.8 | Comparison of TTL and CMOS | 2-7 |
| 2.9 | Comparison of TTL, CMOS and ECL | 2-8 |
| 2.10 | Types of TTL NAND Gates | 2-8 |
| 2.10.1 | The Multiple Emitter Transistor | 2-8 |
| 2.10.2 | Two Input TTL-NAND Gate (Totempole Output) | 2-8 |
| 2.10.3 | Totem-pole (Active Pull up) Output Stage | 2-10 |
| 2.11 | TTL NAND Gate with Open Collector Outputs ... | 2-10 |
| 2.11.1 | Disadvantages of Open Collector Output | 2-11 |
| 2.11.2 | Advantage | 2-11 |
| 2.11.3 | Wired ANDing | 2-11 |
| 2.11.4 | Comparison of Totem-pole and Open Collector Output NAND Gates | 2-12 |



| | |
|---|-------------|
| 2.12 I-Scheme Questions and Answers | 2-13 |
| • Review Questions | 2-12 |

Unit - II

| | |
|--|--------------------|
| Chapter 3 : Combinational Logic Circuits – Part I | |
| | 3-1 to 3-29 |

Syllabus : Standard Boolean representation : Sum of Product (SOP) and Product of Sum (POS), K-map reduction technique for the Boolean expression : Design of arithmetic circuits and code converters using K-map : Half and full adder, Gray to binary and binary to gray (up to 4 bits).

| | |
|---|-----|
| 3.1 Introduction | 3-1 |
| 3.1.1 Classification of Digital Circuits | 3-1 |
| 3.1.2 Combinational Circuit Design | 3-1 |
| 3.1.3 Methods to Simplify the Boolean Equations | 3-1 |
| 3.2 SOP and POS Representations for Logic Expressions | 3-2 |
| 3.2.1 Sum-of-Products (SOP) Form | 3-2 |
| 3.2.2 Product of the Sums Form (POS) | 3-2 |
| 3.2.3 Standard or Canonical SOP and POS Forms | 3-2 |
| 3.2.4 Conversion of a Logic Expression to Standard SOP or POS Form | 3-3 |
| 3.3 Concepts of Minterm and Maxterm | 3-5 |
| 3.3.1 Representation of Logical Expressions using Minterms and Maxterms | 3-6 |
| 3.3.2 Writing SOP and POS Forms for a Given Truth Table | 3-6 |
| 3.3.3 To Write Canonical SOP Expression for a Given Truth Table | 3-6 |

| | |
|---|------|
| 3.3.4 To Write a Canonical POS Expression for a Given Truth Table | 3-7 |
| 3.3.5 Conversion from SOP to POS and Vice Versa | 3-7 |
| 3.4 Methods to Simplify the Boolean Functions | 3-8 |
| 3.4.1 Algebraic Simplification | 3-9 |
| 3.4.2 Disadvantages of Algebraic Method of Simplification | 3-9 |
| 3.5 Karnaugh-Map Simplification | 3-9 |
| 3.5.1 K-map Structure | 3-10 |
| 3.5.2 K-map Boxes and Associated Product Terms | 3-10 |
| 3.5.3 Alternative Way to Label the K-map .. | 3-11 |
| 3.5.4 Truth Table to K-map | 3-11 |
| 3.5.5 Representation of Standard SOP Form on K-map | 3-12 |
| 3.6 K-map Reduction Technique for Boolean Expression | 3-12 |
| 3.6.1 How does Simplification Take Place ? .. | 3-13 |
| 3.6.2 Way of Grouping (Pairs, Quads and Octets) | 3-13 |
| 3.6.3 Grouping Two Adjacent (Pairs) | 3-13 |
| 3.6.4 Grouping Four Adjacent Ones (Quad) | 3-14 |
| 3.6.5 Grouping Eight Adjacent Ones (Octet) | 3-15 |
| 3.6.6 Summary of Rules Followed for K-Map Simplification | 3-16 |
| 3.7 Minimization of SOP Expressions (K-map Simplification) | 3-17 |



| | | |
|--------|---|-------------|
| 3.7.1 | Elimination of a Redundant Group | 3-18 |
| 3.7.2 | Don't Care Conditions | 3-19 |
| 3.7.3 | Disadvantages of K-map Technique | 3-20 |
| 3.8 | Product of Sum (POS) Simplification | 3-20 |
| 3.8.1 | K-map Representation of POS Form | 3-20 |
| 3.8.2 | Representation of Canonical POS Form on K-map | 3-20 |
| 3.9 | Simplification of Canonical POS Form using K-map | 3-21 |
| 3.10 | Design of Arithmetic Circuits | 3-23 |
| 3.11 | Adders | 3-23 |
| 3.11.1 | Half Adder | 3-23 |
| 3.11.2 | Half Adder using Only NAND Gates | 3-23 |
| 3.11.3 | Full Adder | 3-24 |
| 3.11.4 | Full Adder using Half Adders | 3-25 |
| 3.11.5 | Applications of Full Adder | 3-25 |
| 3.11.6 | Comparison of Half Adder and Full Adder | 3-25 |
| 3.12 | Code Converters | 3-26 |
| 3.12.1 | Binary to Gray Code Converter | 3-26 |
| 3.12.2 | Gray to Binary Code Conversion | 3-27 |
| 3.13 | I-Scheme Solved Examples..... | 3-29 |
| 3.14 | I-Scheme Questions and Answers | 3-29 |
| • | Review Questions | 3-28 |

Unit - II**Chapter 4 : Combinational Logic Circuits – Part II**
4-1 to 4-16

Syllabus : Multiplexer and Demultiplexer : Working, Truth
table and applications of multiplexers and demultiplexers.

| | | |
|-------|---|------|
| 4.1 | Multiplexer (Data Selector) | 4-1 |
| 4.1.1 | Need of Multiplexers | 4-1 |
| 4.1.2 | Advantages of Multiplexers | 4-2 |
| 4.2 | Types of Multiplexers | 4-2 |
| 4.2.1 | 2 : 1 Multiplexer | 4-2 |
| 4.2.2 | A 4 : 1 Multiplexer | 4-2 |
| 4.2.3 | 8 : 1 Multiplexer | 4-3 |
| 4.2.4 | 16 : 1 MUX | 4-3 |
| 4.3 | Applications of a Multiplexer | 4-4 |
| 4.4 | Multiplexer Tree | 4-4 |
| 4.5 | Use of Multiplexers in Combinational Logic Design | 4-5 |
| 4.5.1 | Implementing a Canonical POS Expression using Multiplexer | 4-10 |
| 4.5.2 | Implementation of Boolean SOP Expression with Don't Care Conditions | 4-10 |
| 4.6 | Demultiplexers | 4-11 |
| 4.6.1 | Demultiplexer Principle | 4-11 |
| 4.7 | Types of Demultiplexers | 4-11 |
| 4.7.1 | 1 : 2 Demultiplexer | 4-11 |
| 4.7.2 | 1 : 4 Demultiplexer | 4-12 |
| 4.7.3 | 1 : 8 Demultiplexer | 4-13 |
| 4.7.4 | 1 : 16 Demultiplexer | 4-13 |
| 4.8 | Demultiplexer Tree | 4-13 |
| 4.8.1 | Comparison of Multiplexer and Demultiplexer | 4-15 |
| 4.8.2 | Use of DEMUX in Combinational Logic Design | 4-15 |



| | | |
|-------|--------------------------------------|------|
| 4.8.3 | Applications of Demultiplexer | 4-16 |
| 4.9 | I-Scheme Questions and Answers | 4-16 |
| • | Review Questions | 4-16 |

Unit - II

| | |
|-------------------------------|--------------------|
| Chapter 5 : Flip Flops | 5-1 to 5-19 |
|-------------------------------|--------------------|

Syllabus : Basic memory cell : RS-latch using, NAND and NOR, SR flip flops : SR-flipflop, Clocked SR flip flop with preset and clear, Drawbacks of SR flip flop. JK flip flops : Clocked JK flip flop with preset and clear, Master slave JK flip flop, D and T type flip flop, Excitation table of flip flops.

| | | |
|-------|---|-----|
| 5.1 | Introduction to Sequential Logic Circuits | 5-1 |
| 5.1.1 | Combinational Circuits | 5-1 |
| 5.1.2 | Sequential Circuits | 5-1 |
| 5.1.3 | Comparison of Combinational and Sequential Circuits | 5-1 |
| 5.2 | Clock Signal | 5-2 |
| 5.3 | Latches | 5-2 |
| 5.3.1 | 1-Bit Memory Cell (Cross Coupled Inverter) | 5-2 |
| 5.4 | RS Latch | 5-2 |
| 5.4.1 | S-R Latch using NOR Gates | 5-2 |
| 5.4.2 | S-R Latch using NAND Gates | 5-4 |
| 5.5 | Triggering Methods | 5-5 |
| 5.5.1 | Difference between Latch and Flip-flop | 5-5 |
| 5.5.2 | Level Triggering | 5-6 |
| 5.5.3 | Types of Level Triggered Flip-flops | 5-6 |
| 5.5.4 | Edge Triggering | 5-6 |
| 5.5.5 | Types of Edge Triggered Flip Flops | 5-6 |

| | | |
|--------|--|------|
| 5.6 | Clocked SR Flip Flops | 5-6 |
| 5.6.1 | Positive Edge Triggered SR Flip Flop | 5-6 |
| 5.6.2 | Negative Edge Triggered S - R Flip Flop | 5-7 |
| 5.6.3 | Drawback of S-R Flip Flop | 5-8 |
| 5.7 | Clocked D Flip-flop | 5-8 |
| 5.7.1 | Positive Edge Triggered D Flip-flop | 5-8 |
| 5.7.2 | Negative Edge Triggered D Flip Flop | 5-9 |
| 5.7.3 | Applications of D Flip-flop | 5-9 |
| 5.8 | Edge Triggered (Clocked) J-K Flip Flop | 5-9 |
| 5.8.1 | Positive Edge Triggered JK Flip Flop ... | 5-10 |
| 5.8.2 | Negative Edge Triggered JK Flip-Flop . | 5-11 |
| 5.9 | Level Triggered JK Flip Flop or JK Latch | 5-11 |
| 5.9.1 | Race Around Condition in Level Triggered JK FF | 5-12 |
| 5.9.2 | How does an Edge Triggered JK FF Avoid Race Around Condition ? | 5-12 |
| 5.10 | Toggle Flip Flop (T Flip Flop) | 5-13 |
| 5.10.1 | Positive Edge Triggered T-FF | 5-13 |
| 5.10.2 | Negative Edge Triggered T Flip Flop ... | 5-14 |
| 5.10.3 | Application of T FF | 5-14 |
| 5.11 | Master Slave (MS) JK Flip Flop | 5-15 |
| 5.12 | Clocked FFs with Preset and Clear Inputs | 5-16 |
| 5.12.1 | S-R Flip-Flop with Preset and Clear Inputs | 5-16 |
| 5.12.2 | JK Flip Flop with Preset and Clear Inputs | 5-17 |
| 5.13 | Excitation Table of Flip-Flop | 5-17 |



| | | |
|---------------------------------|--|-------------|
| 5.13.1 | Excitation Table of SR Flip Flops | 5-17 |
| 5.13.2 | Excitation Table of D Flip Flop | 5-18 |
| 5.13.3 | Excitation Table of JK Flip Flop | 5-18 |
| 5.13.4 | Excitation Table of T Flip Flop | 5-18 |
| 5.14 | Conversion of Flip Flops | 5-18 |
| 5.15 | Applications of Flip Flops | 5-18 |
| 5.16 | Comparisons | 5-19 |
| 5.16.1 | Comparison of D Flip-flop and T Flip-flop | 5-19 |
| 5.16.2 | Comparison of SR Flip-flop and JK Flip-flop | 5-19 |
| 5.17 | I-Scheme Questions and Answers | 5-19 |
| • Review Questions | | 5-19 |

Unit - II

| | |
|-----------------------------|--------------------|
| Chapter 6 : Counters | 6-1 to 6-12 |
|-----------------------------|--------------------|

Syllabus : Asynchronous counter, Synchronous counter.

| | | |
|-------|--|-----|
| 6.1 | Introduction | 6-1 |
| 6.1.1 | Types of Counters | 6-1 |
| 6.1.2 | Classification of Counters | 6-1 |
| 6.2 | Asynchronous Up Counters | 6-1 |
| 6.2.1 | 3 Bit Asynchronous Up Counter | 6-1 |
| 6.2.2 | 4 Bit Asynchronous Up Counter | 6-3 |
| 6.2.3 | State Diagram of a Counter | 6-4 |
| 6.2.4 | Modulus of the Counter | 6-4 |
| 6.2.5 | Frequency Division in Asynchronous Counters | 6-4 |
| 6.3 | Asynchronous Down Counter | 6-6 |
| 6.3.1 | 3-Bit Asynchronous Down Counter | 6-6 |

| | | |
|---------------------------------|--|-------------|
| 6.4 | Disadvantages of Ripple Counters | 6-9 |
| 6.5 | Synchronous Up Counters | 6-9 |
| 6.5.1 | 2-Bit Synchronous Up Counter | 6-9 |
| 6.5.2 | 3-Bit Synchronous Binary Up Counter | 6-10 |
| 6.5.3 | Synchronous Counter using T Flip Flops | 6-11 |
| 6.5.4 | Four Bit Synchronous Up Counter | 6-11 |
| 6.5.5 | Advantages of Synchronous Counter .. | 6-12 |
| 6.5.6 | Comparison of Synchronous and Asynchronous Counters | 6-12 |
| 6.6 | Applications of Counters | 6-12 |
| 6.7 | I-Scheme Questions and Answers | 6-12 |
| • Review Questions | | 6-12 |

UNIT - III

| | |
|--|--------------------|
| Chapter 7 : Basics of Microprocessor and 8051 | |
| Microcontroller | 7-1 to 7-25 |

Syllabus : Microprocessor, Microcomputers and Microcontrollers (Basic introduction and comparison), Types of buses, address bus, data bus and control bus, Harvard and Von-Neumann architecture, 8051 Microcontroller architecture, Pin configuration, stack, memory organization, Boolean processor, Power Saving Options-Idle and power down mode, Comparison between Derivatives of 8051 (8951, 8952, 8031, 8751).

| | | |
|-------|---|-----|
| 7.1 | Basics of Microprocessor, Microcomputer, Microcontroller | 7-1 |
| 7.1.1 | Microprocessor | 7-1 |
| 7.1.2 | Microcomputer | 7-2 |
| 7.1.3 | Microcontroller | 7-2 |



| | |
|---|---|
| 7.1.4 Comparison between Microprocessor, Microcontroller and Microcomputer 7-4 | 7.5.4 Difference between Power down and Idle Mode 7-22 |
| 7.2 Types of Buses 7-4 | 7.6 Derivatives of 8051 7-23 |
| 7.3 Types of Architectures 7-4 | 7.7 Comparison between 8031, 8051 and 8751 7-24 |
| 7.3.1 Von Neumann's Architecture 7-4 | 7.8 I-Scheme Questions and Answers 7-24 |
| 7.3.2 Harvard Architecture 7-5 | UNIT - IV |
| 7.3.3 Difference between Harvard and Von Neumann Architecture 7-5 | Chapter 8 : 8051 Instruction Set and Programming 8-1 to 8-62 |
| 7.4 8051 Microcontroller 7-5 | Syllabus : Addressing modes, Instruction set (Data Transfer, Logical, Arithmetic, Branching, Machine Control, Stack operation, Boolean), Assembly language programming (ALP), Software development cycle - Editor, Assembler, cross compiler, linker, locator, compiler, Assembler directives - ORG, DB, EQU, END, CODE, DATA. |
| 7.4.1 Features of 8051 7-6 | 8.1 Introduction 8-1 |
| 7.4.2 Pin Diagram of 8051 7-6 | 8.2 Addressing Modes of 8051 8-1 |
| 7.4.3 Pin Description of 8051 7-6 | 8.2.1 Immediate Addressing 8-1 |
| 7.4.4 Oscillator Characteristics 7-8 | 8.2.2 Direct Addressing 8-1 |
| 7.4.5 Architecture of 8051 7-8 | 8.2.3 Indirect Addressing (Register Indirect) ... 8-2 |
| 7.4.6 8051 Registers 7-9 | 8.2.4 Register Addressing 8-2 |
| 7.4.7 Counters and Timers Registers 7-15 | 8.2.5 External Direct Addressing 8-2 |
| 7.4.8 Serial Communication Registers 7-19 | 8.2.6 External Indirect Addressing 8-2 |
| 7.4.9 PCON (Power Control, Addresses 87H) 7-20 | 8.3 Group of Instruction Set 8-3 |
| 7.4.10 Memory Organization in 8051 7-20 | 8.3.1 Data Transfer Instructions 8-3 |
| 7.4.10(A) Program Memory 7-20 | 8.3.2 Arithmetic Instructions 8-6 |
| 7.4.10(B) Data Memory 7-20 | 8.3.3 Logical Instructions 8-11 |
| 7.4.10(C) Stack in 8051 Microcontroller 7-21 | 8.3.4 Stack Instructions 8-14 |
| 7.5 8051 Boolean Processor 7-21 | 8.3.5 Branching and Machine Control |
| 7.5.1 Power Saving Options 7-22 | Instructions 8-15 |
| 7.5.2 Idle Mode 7-22 | |
| 7.5.3 Power down Mode 7-22 | |



| | |
|--|--|
| 8.3.6 Boolean Operation Instructions8-19 | 8.6.11 Smallest Number Among the Block / Array Stored in External Memory8-42 |
| 8.4 Program Development Steps8-23 | 8.6.12 Arrange Numbers in Descending Order8-43 |
| 8.4.1 Defining the Problem8-23 | 8.6.13 Arrange Numbers in Ascending Order8-44 |
| 8.4.2 Algorithm8-23 | 8.6.14 Block Transfer in Internal Memory8-46 |
| 8.4.3 Flowchart8-23 | 8.6.15 Count ODD Numbers in Block of N Number Stored in External RAM8-47 |
| 8.4.4 Initialization Checklist8-23 | 8.6.16 Count EVEN Numbers in Block of N Number Stored in External RAM8-48 |
| 8.4.5 Choosing Instructions8-23 | 8.6.17 Count Positive Numbers in Block of N Number Stored in External RAM8-49 |
| 8.4.6 Converting Algorithms to Assembly Language Program8-23 | 8.6.18 Count Negative Numbers in Block of N Number Stored in External RAM8-50 |
| 8.5 Elements of Assembler8-23 | 8.6.19 2 nd Complement of the Number8-51 |
| 8.5.1 Syntax of Assembly Language8-23 | 8.6.20 Addition of Two BCD Numbers8-52 |
| 8.5.2 Operators8-25 | 8.6.21 Count '0' and '1' in 8 Bit Number8-55 |
| 8.5.3 Symbols8-25 | 8.6.22 Program to Unpacked 8 Bit Number8-57 |
| 8.5.4 Labels8-26 | 8.7 Software Development Cycle8-58 |
| 8.6 Assembly Language Programming8-26 | 8.7.1 Writing Microcontroller Code8-58 |
| 8.6.1 Addition of Two 8 Bit Numbers8-26 | 8.7.2 Translating the Source Code to Machine Code8-59 |
| 8.6.2 Addition of Two 16 Bit Numbers8-29 | 8.7.3 Debugging the Code8-59 |
| 8.6.3 Sum of Series of 8 Bit Numbers8-30 | 8.7.4 Flash Programming8-59 |
| 8.6.4 Subtraction of Two 8 Bit Numbers8-33 | 8.8 Software Development Tools8-60 |
| 8.6.5 Subtraction of Two 16 Bit Numbers8-34 | 8.8.1 Editor8-60 |
| 8.6.6 Multiplication of Two 8 Bit Numbers8-35 | 8.8.2 Assembler8-60 |
| 8.6.7 Division of Two 8 Bit Numbers8-37 | 8.8.3 Cross Compiler8-60 |
| 8.6.8 Largest Among the Block / Array Stored in Internal Memory8-39 | |
| 8.6.9 Smallest Number among the Block / Array Stored in Internal Memory8-40 | |
| 8.6.10 Largest Number among the Block / Array Stored in External Memory8-41 | |



| | | |
|-------|--------------------------------------|------|
| 8.8.4 | Linker | 8-60 |
| 8.8.5 | Locator | 8-60 |
| 8.8.6 | Compiler | 8-60 |
| 8.9 | Assembler Directives | 8-61 |
| 8.9.1 | EQU Directive | 8-61 |
| 8.9.2 | CODE Directive | 8-61 |
| 8.9.3 | DATA Directive | 8-61 |
| 8.9.4 | ORG Directive | 8-61 |
| 8.9.5 | END Directive | 8-61 |
| 8.9.6 | DB : Define Byte | 8-61 |
| 8.10 | I-Scheme Solved Examples..... | 8-61 |
| 8.11 | I-Scheme Questions and Answers | 8-62 |

UNIT - V**Chapter 9 : 8051 Memory Device Interfacing and Application** **9-1 to 9-28**

Syllabus : Memory interfacing : Program and Data Memory, I/O Interfacing : LED, Relays, Keyboard, LCD, Seven Segment display, stepper motor, Square Wave generation using port pins of 8051. Water level controller, Stepper motor control for clockwise and anticlockwise rotation, Traffic light controller.

| | | |
|----------|--|-----|
| 9.1 | Memory Interfacing | 9-1 |
| 9.1.1 | Introduction | 9-1 |
| 9.1.2 | Semiconductor Memory | 9-1 |
| 9.1.3 | Different Memory IC's Available | 9-2 |
| 9.1.4 | Address Decoding | 9-2 |
| 9.1.5 | Absolute and Linear Decoding Techniques | 9-3 |
| 9.1.5(A) | Absolute Decoding | 9-3 |

| | | |
|----------|--|------|
| 9.1.5(B) | Linear Decoding | 9-3 |
| 9.1.5(C) | Difference between Absolute and Linear Decoding | 9-3 |
| 9.1.6 | Data, Address and Control Bus of 8051 . | 9-3 |
| 9.1.7 | Interfacing of $8K \times 8$ Program ROM | 9-4 |
| 9.1.8 | Interfacing of $8K \times 8$ Data ROM | 9-4 |
| 9.1.9 | Interfacing of $8K \times 8$ Data ROM and $8K \times 8$ Program ROM | 9-5 |
| 9.1.10 | Interfacing of $8K \times 8$ Data RAM | 9-6 |
| 9.1.11 | Interfacing of 64K External RAM and ROM | 9-6 |
| 9.1.12 | Interfacing of 4KB RAM and 4KB EPROM | 9-6 |
| 9.1.13 | Interfacing of $2K \times 8$ Data RAM | 9-7 |
| 9.2 | I/O Interfacing | 9-7 |
| 9.2.1 | Interfacing of LED (Light Emitting Diode) with 8051 | 9-7 |
| 9.2.2 | Interfacing of 8 LEDs with 8051 Ports | 9-8 |
| 9.2.3 | Seven Segment Display | 9-9 |
| 9.2.3(A) | Interfacing Seven Segment Display to 8051 | 9-9 |
| 9.2.3(B) | Interfacing Multiplexed 7 Segment Display with 8051 (4 Digit) | 9-10 |
| 9.2.4 | 4 × 4 Matrix Keyboard | 9-11 |
| 9.2.4(A) | Interfacing of 4 × 4 Matrix Keyboard | 9-11 |
| 9.2.4(B) | Algorithm | 9-11 |
| 9.2.4(C) | Flowchart..... | 9-12 |
| 9.2.4(D) | Program | 9-12 |



| | |
|---|---|
| 9.2.5 Interfacing of Relays with 8051 Port9-13 | 9.2.7 Interfacing of Stepper Motor with 80519-18 |
| 9.2.6 LCD (Liquid Crystal Display)9-14 | |
| 9.2.6(A) Basics of LCD9-14 | 9.3 Square Wave Generation using Port Pins of 80519-18 |
| 9.2.6(B) LCD Initialization9-14 | 9.4 Water Level Controller9-22 |
| 9.2.6(C) Interfacing of 2 x 16 LCD9-15 | 9.5 Stepper Motor Rotation Control9-23 |
| 9.2.6(D) Initializing and Sending Data to the LCD9-15 | 9.6 Traffic Light Controller using 80519-25 |
| 9.2.6(E) Program to display "WELCOME" to LCD Character9-16 | 9.7 I-Scheme Solved Examples9-26 |
| 9.2.6(F) Interfacing 20 x 4 LCD with 80519-17 | 9.8 I-Scheme Questions and Answers9-27 |
| | • List of PracticalsL-1 to L-14 |



List of Practicals

| Sr. No. | Practical Statement | Page No. |
|--------------|---|----------|
| Practical 1 | Identify the various blocks of 8051 microcontroller. | L-1 |
| Practical 2 | Write an assembly language program to perform arithmetic operation on 8 bit such as addition, subtraction, multiplication and division. | L-1 |
| Practical 3 | Write an assembly language program to transfer data from source to destination location of internal data memory. | L-8 |
| Practical 4 | Write an assembly language program to transfer data from source to destination location of external data memory. | L-9 |
| Practical 5 | Write an assembly language program to exchange data from source to destination location. | L-10 |
| Practical 6 | Interface LED with microcontroller to turn ON the LED. | L-11 |
| Practical 7 | Interface 7 segment display to display decimal number from 0 to 9. | L-12 |
| Practical 8 | Interface the given keyboard with 8051 and display the key pressed. | L-12 |
| Practical 9 | Interface LCD with 8051 microcontroller to display the character and decimal digit. | L-13 |
| Practical 10 | Interface stepper motor to microcontroller and rotate in clockwise and anti-clockwise direction at given angle. | L-14 |

